UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/805,136	03/19/2004	Matthew F. Davis	8381/ETCH/SILICON/JB1	8916

55649 7590 02/07/2006

MOSER IP LAW GROUP / APPLIED MATERIALS, INC.
1040 BROAD STREET
2ND FLOOR
SHREWSBURY, NJ 07702

EXAMINER	
DAHIMENE, MAHMOUD	

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 02/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/805,136	DAVIS ET AL.	
	Examiner	Art Unit	
	Mahmoud Dahimene	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21 and 28-52* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *22-27* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/20/04 and 12/23/04*
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-21 and 28-52, drawn to a method, classified in class 216, subclass 59.

II. Claims 22-27, drawn to an apparatus, classified in class 365, subclass 1+.

The inventions are distinct, each from the other because of the following reasons:

Inventions I and II are related as process and apparatus for its practice. The inventions are distinct if it can be shown that either: (1) the process as claimed can be practiced by another materially different apparatus or by hand, or (2) the apparatus as claimed can be used to practice another and materially different process. (MPEP § 806.05(e)). In this case the process as claimed can be practiced by another materially different apparatus or by entering data by hand.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

During a telephone conversation with Alan Taboada on 1/27/06 a provisional election was made with traverse to prosecute the invention of group I, claims 1-21 and 28-52. Affirmation of this election must be made by applicant in replying to this Office

action. Claims 22-27 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 11 and 45 recite the limitation "the processing equipment" and "the processing system" in pages 24 and 29. There is insufficient antecedent basis for these limitations in the claims.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 28-35 are rejected under 35 U.S.C. 102(e) as being anticipated by Fairbairn et al. (US 6,625,497).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

The reference of Fairbairn et al. discloses a semiconductor processing module with integrated feedback/feed forward metrology wherein a method of controlling a process of fabricating integrated devices is described, the method comprises:

measuring a pre-etch dimension (CD) (column 4, line 42) and a post-etch CD (column 12, line 25) of at least one structure on a substrate and

Adjusting a process recipe on an etch process (column 11, line 62) and enabling feedback to the photocell (lithography) (column 5, line 53) (column 10, line 64) or possibly photoresist trimming or shrinking (column 13, line 44) which are a capabilities for adjusting a process recipe of a pre-etch process.

As to claims 28-30, the reference of Fairbairn et al. discloses "In a further embodiment of the present invention illustrated in FIG. 8, a process identical to that described above with reference to FIG. 7 is carried out, except that after the etched features CD is measured at step 770, the data is fed back to update a process model

M2 to select an etch recipe for subsequently processed wafers at step 880. In a still further embodiment of the present invention, feature CD data acquired at step 770 is also fed back to update process model M1 to adjust the trim recipe for subsequently processed wafers at step 730" (column 13, line 65). It is suggested that in an extreme case, feature CD data 770 can be fed-back to model M1 to cancel resist trim 740 if the feature CD 770 meets the targeted value with no photoresist trimming thereby adjusting the process sequence in response to process measurement data 770.

As to claims 31-35 the reference Fairbairn et al. cites "Of course, the cleaning and/or further inspection steps described above available at the apparatus of Figs. 9B and 9C can be performed as appropriate and/or desired" (column 14, line 13). The "further inspection" could be a CD measurement for verification triggered by a control system fault which is usually unscheduled. The cleaning step (referred to above in this paragraph) is a fabrication step.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein

were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 2-5, 8-17 are rejected under 35 U.S.C. 103(a) as being obvious over Fairbairn et al. (US 6,625,497) as applied to claims 1, 28-35 above, and further in view of Krivokapic et al. (US 6,567,717).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing

that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

The reference of Fairbairn et al. is silent about executing a mulpti-pass process.

Krivokapic et al. disclose a semiconductor feed-forward control process wherein "non-conforming post-etch wafers may be returned for further etching if under-etched" (column 10, line 35).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Fairbairn et al. allowing an under-etched wafer to be re-processed or re-etched one or more times as needed until the desired etch result is obtained, the post-etched process of CD measurement will be repeated as well to compare results with a desired CD characteristics, because the reference of Krivokapic et al. teaches that if a wafer is under-etched it can be re-etched. One of ordinary skill in the art, given the capability of immediate post-etched CD measurements, would have been motivated to re-etch an under-etched wafer in order to reduce manufacturing cost associated with either discarding the wafer or proceeding to final tests.

As to claim 3, one of ordinary skill in the art would have been motivated to search and detect a failure of processing equipment if the modified method of Fairbairn et al. yields post-etch CD measurements that are consistently out of specification. Equipment failure detection is a routine procedure when a process fault is detected, otherwise manufacturing yield will be greatly affected.

As to claims 4, the reference of Fairbairn et al. discloses "Further exemplary embodiments of the present invention can be implemented. In these embodiments CD at the resist trim and feature etch processes (such as gate etch, shallow trench isolation (STI) trench etch, via etch, contact hole etch, metal etch, etc.) is tightly controlled using feedback and feed forward of CD measurement in real time under controlled environmental conditions" (column 13, lines 14-22). As an example a typical dual-damascene via etch is performed on a substrate including a photoresist layer, a BARC layer, a low-k dielectric, and an etch stop layer. After the BARC open step, the substrate would consist of a photoresist featured layer and a film stack (photoresist and BARC) having at least a featured layer, and a low-k blanket layer, and a film stack (low-k and etch-stop layer) having at least one blanket layer.

As to claim 5, the CD measurements suggested by Fairbairn et al., such as CD-SEM or optical inspection tool (column 4, line 58), are non-destructive measurements.

As to claim 8, Fairbairn et al. discloses a CD measurement ex-situ to the etch chamber (figure 9A-9C).

As to claims 9 and 10, a CD-SEM measures topographic dimensions in the same processing system including the etch chamber (figures 9A-C).

As to claim 11, the examiner's interpretation of this claim is: The method of claim 1, wherein the ~~processing~~ measuring equipment is external to the processing system. Fairbairn et al. disclose external CD measurement is conventional in the art (column 2, line 40).

As to claim 12, Fairbairn et al. describes in the "background art" section a method where the results of CD measurements are then used to adjust the etch recipe for the remaining wafers in the lot which is at least one subsequent substrate (column 3, line 6).

As to claim 13, one pre-etch process is considered to be the photo cell exposure in the method of Fairbairn et al. (column 4, line 60) performed before pre-etch dimension measurement

As to claim 14, the reference of Fairbairn et al. describes a post etch cleaning (911) process (column 4, line 48) which could be performed after measuring the post etch measurement.

As to claim 15, the reference of Fairbairn et al. describes a lithographic step performed as a pre-etch process (column 4, line 42).

As to claim 16, the reference of Fairbairn et al. describes a a processing system including an etch chamber and a CD measurement unit (figures 9A-9C)

As to claim 17, the reference of Fairbairn et al. an external CD measurement is conventional in the art (column 2, line 40).

9. Claims 6, 7 and 18 are rejected under 35 U.S.C. 103(a) as being obvious over Fairbairn et al. (US 6,625,497) as applied to claims 1, 28-35 above, and further in view of Perry et al. (US 2004/0087041).

It is noted that the reference of Fairbairn et al. is silent about a measuring step which is performed in-situ within the etch chamber, however, the reference teaches the

benefit of performing the etch and measurement within the same controlled environment thereby increasing throughput and improving yield.

The reference of Perry et al. describes an in-situ method for controlling a recess etch process wherein interferometry is used to monitor the initial thickness of a top layer or the actual etching of the recess in real time in an etch chamber (pages 3 and 4 , paragraphs 0039 and 0055), the measurement system comprises a process module, data collection and a computer (figure 4A). The interferometry measurement is also conventionally used as an end-point detection.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify the method of Fairbairn et al. by including the etch chamber in-situ measurement system of Perry et al. because etch recess measurement is as important as CD measurement particularly when it is performed within the etch chamber for manufacturing process control and reliability of the final product. One of ordinary skill in the art would have been motivated to use an etch recess measurement for process controllability in order to detect under-etching or over-etching before the wafer leaves the etched chamber.

10. Claims 19-21 are rejected under 35 U.S.C. 103(a) as being obvious over Fairbairn et al. (US 6,625,497) as applied to claims 1, 28-35 above, and further in view of Morgenstern (US 2003/0022510)

The reference of Fairbairn et al. discloses a trench etch (column 13, lines 14-22), but fails to specifically disclose a trench capacitor.

The reference of Morgenstern (US 2003/0022510) teaches a formation of a capacitive trench structure with a polysilicon electrode layer wherein the etch process is performed with an HBr and Cl2 chemistry (page 2, paragraphs 0033-0035). The flow rate of HBr:Cl2 is 45:135 or 1:3 (page 3, paragraph 0044).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify the method of Fairbairn et al. by including a capacitive trench structure with a polysilicon electrode layer wherein the etch process is performed with an HBr and Cl2 chemistry because the reference of Fairbairn et al. teaches the disclosed control method is applicable to any structure. One of ordinary skill in the art would be motivated to apply the method of Fairbairn et al. to a capacitive structure in order to control the capacitance characteristics and values with a high precision from wafer-to-wafer in a manufacturing environment.

11. Claims 36-52 are rejected under 35 U.S.C. 103(a) as being obvious over Fairbairn et al. (US 6,625,497) as applied to claims 1, 28-35 above in view of Krivokapic et al. (US 6,567,717), and further in view of Perry et al. (US 2004/0087041).

It is noted that the reference of Fairbairn et al., described above, is silent about a multi-pass process. Krivokapic et al. disclose a semiconductor feed-forward control process wherein "non-conforming post-etch wafers may be returned for further etching if under-etched" (column 10, line 35), which in effect describes a multi-pass process.

/

Perry et al. disclose a control etch method based on an in-situ thickness measurement step.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Fairbairn et al. to include the thickness measurement method of Perry et al. allowing wafers which are detected to be under-etched by a post-etch measurement step to be sent back to (or remain in) the etcher for additional etching with duration determined from the differential thickness between the measured etched depth and the target etch depth, or in the method of Fairbairn et al. the CD measurement can be compared to the target waveform and if not matched, the wafer can be re-processed to match the desired profile, the process can be repeated more than once if necessary, because the methods of Krivokapic et al. and that of Perry et al. when combined with the method of Fairbairn et al. will result in further increase of yield and decrease of production cost as initially suggest by Fairbairn et al. when discussing the benefits of feedback and feed-forward controls (column 13, line 8). One of ordinary skill in the art would have been motivated to include a multi-pass process to the control method of Fairbairn et al. in order to be able to insure process performance including the instance where some of the substrate parameters have been change (e.g. previously deposited film quality), the controlled multi-pass method would be able to correct for such changes by automatic inspection and process adjustments.

As to claim 37, it would be obvious to one of ordinary skill in the art to expect some kind of a failure if the target CD waveform or depth is not achieved after the final

inspection step . Detecting equipment failure would be the first obvious trouble-shooting step.

As to claim 38, see discussion about claim 4 above.

As to claim 39, none of the measurements cited in the references above are destructive.

As to claim 40, Perry et al. disclose an in-situ measurement method, see discussion for claim 6 above.

As to claim 41, see discussion for claim 7 above.

As to claim 42, see discussion for claim 8 above.

As to claim 43, see discussion for claim 9 above.

As to claim 44, see discussion for claim 10 above.

As to claim 45, see discussion for claim 11 above.

As to claim 46, see discussion for claim 12 above.

As to claim 47, see discussion for claim 13 above.

As to claim 48, see discussion for claim 14 above.

As to claim 49, see discussion for claim 15 above.

As to claim 50, see discussion for claim 16 above.

As to claim 51, see discussion for claim 17 above.

As to claim 52, see discussion for claim 18 above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mahmoud Dahimene whose telephone number is (571) 272-2410. The examiner can normally be reached on week days from 8:00 AM. to 5:00 PM..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on (571) 272-1465. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mahmoud Dahimene

MD

NADINE G. NORTON
SUPERVISORY PATENT EXAMINER